ABSTRACT

A semiconductor memory such as a dynamic RAM having memory mats each divided into a plurality of units or sub-memory mats. Each sub-memory mat comprises: a memory array having sub-word lines and sub-bit lines intersecting orthogonally and dynamic memory cells located in lattice fashion at the intersection points between the intersecting sub-word and sub-bit lines; a sub-word line driver including unit sub-word line driving circuits corresponding to the sub-word lines; a sense amplifier including unit amplifier circuits and column selection switches corresponding to the sub-bit lines; and sub-common I/O lines to which designated sub-bit lines are connected selectively via the column selection switches. The sub-memory mats are arranged in lattice fashion. Above the sub-memory mats is a layer of: main word lines and column selection signal lines intersecting orthogonally, the main word lines having a pitch that is an integer multiple of the pitch of the sub-word lines, the column selection signal lines having a pitch that is an integer multiple of the pitch of the sub-bit lines; and main common I/O lines to which designated sub-common I/O lines are connected selectively.